



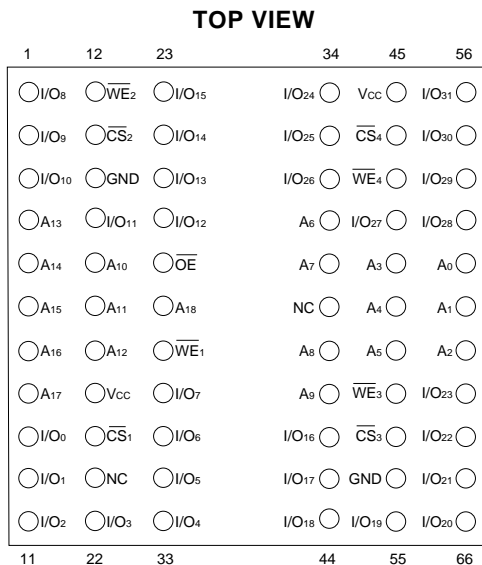
512Kx32 SRAM MODULE, SMD 5962-94611 PRELIMINARY*

FEATURES

- Access Times of 70, 85, 100, 120ns
- Packaging
 - 66-pin, PGA Type, 1.185 inch square, Hermetic Ceramic HIP (Package 401)
 - 66-pin, PGA Type, 1.385 inch square, Hermetic Ceramic HIP (Package 402)
 - 68 lead, 40mm Hermetic Low Profile CQFP, 3.56mm (0.140"), (Package 502)
 - 68 lead, Hermetic CQFP, 22.4mm (0.880 inch) square. Designed to fit JEDEC 68 lead 0.990" CQFJ footprint.
 - G2 (Package 500), 5.08mm (0.200 inch) high
 - G2T (Package 509), 4.57mm (0.180 inch) high
- Organized as 512Kx32, User Configurable as 1024Kx16 or 2Mx8
- Commercial, Industrial and Military Temperature Ranges
- TTL Compatible Inputs and Outputs
- 5 Volt Power Supply
- Low Power CMOS
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
 - WS512K32-XG2X - 8 grams typical
 - WS512K32-XG2TX - 8 grams typical
 - WS512K32-XHX - 13 grams typical
 - WS512K32-XH2X - 13 grams typical
 - WS512K32-XG4TX - 20 grams typical

* This data sheet describes a product under development, not fully characterized, and is subject to change without notice.

FIG. 1 PIN CONFIGURATION FOR WS512K32-XHX



PIN DESCRIPTION

I/O ₀₋₃₁	Data Inputs/Outputs
A ₀₋₁₈	Address Inputs
WE ₁₋₄	Write Enables
CS ₁₋₄	Chip Selects
OE	Output Enable
V _{CC}	Power Supply
GND	Ground
NC	Not Connected

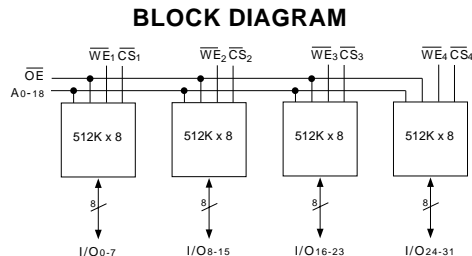
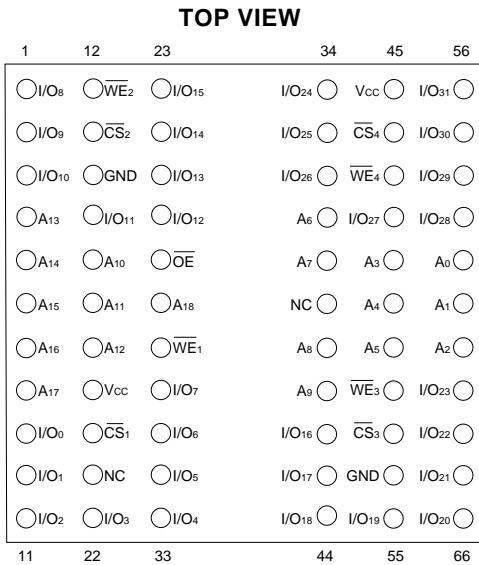




FIG. 2 PIN CONFIGURATION FOR WS512K32N-XH2X



PIN DESCRIPTION

I/O ₀₋₃₁	Data Inputs/Outputs
A ₀₋₁₈	Address Inputs
\overline{WE}_{1-4}	Write Enables
\overline{CS}_{1-4}	Chip Selects
\overline{OE}	Output Enable
V _{CC}	Power Supply
GND	Ground
NC	Not Connected

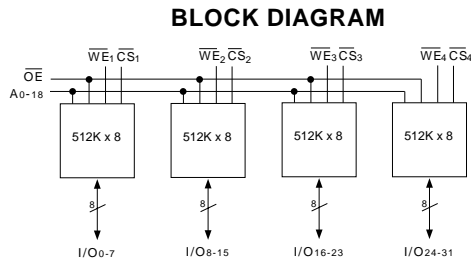
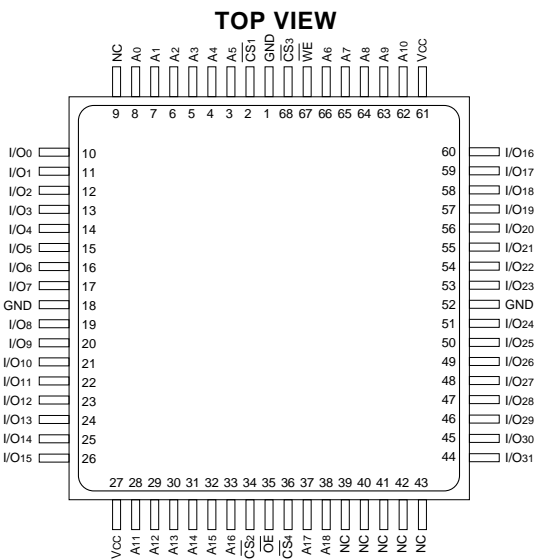


FIG. 3 PIN CONFIGURATION FOR WS512K32-XG4TX Low Profile



PIN DESCRIPTION

I/O ₀₋₃₁	Data Inputs/Outputs
A ₀₋₁₈	Address Inputs
\overline{WE}	Write Enable
\overline{CS}_{1-4}	Chip Selects
\overline{OE}	Output Enable
V _{CC}	Power Supply
GND	Ground
NC	Not Connected

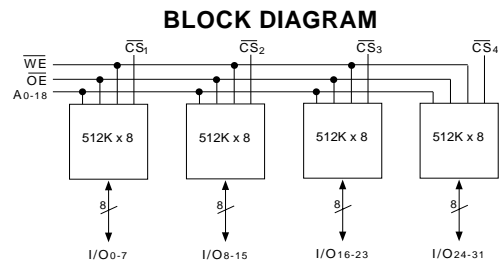
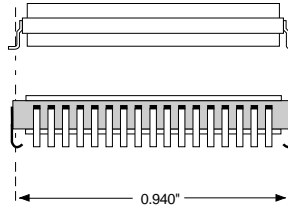
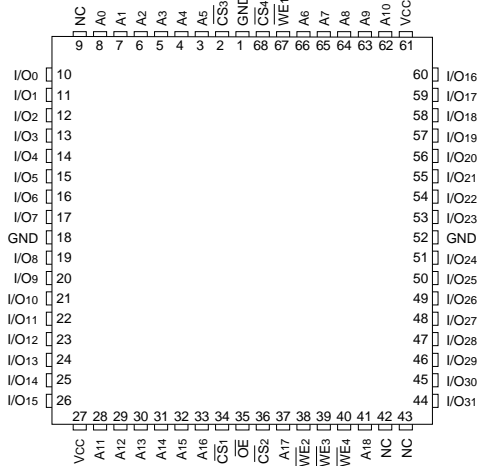




FIG. 4 PIN CONFIGURATION FOR WS512K32-XG2X AND WS512K32-XG2TX

TOP VIEW

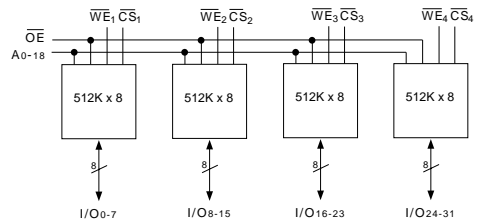


The White 68 lead G2/G2T CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2/G2T has the TCE and lead inspection advantage of the CQFP form.

PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-18	Address Inputs
WE1-4	Write Enables
CS1-4	Chip Selects
OE	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _G	-0.5	V _{CC} +0.5	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	7.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	4.5	5.5	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.5	+0.8	V
Operating Temp (Mil)	T _A	-55	+125	°C

TRUTH TABLE

\overline{CS}	\overline{OE}	\overline{WE}	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	H	H	Out Disable	High Z	Active
L	X	L	Write	Data In	Active

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
OE capacitance	C _{OE}	V _{IN} = 0 V, f = 1.0 MHz	50	pF
\overline{WE} 1-4 capacitance HIP (PGA) COFP G4 COFP G2 COFP G2T	C _{WE}	V _{IN} = 0 V, f = 1.0 MHz	20 50 20 15	pF
\overline{CS} 1-4 capacitance	C _{CS}	V _{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	C _{I/O}	V _{I/O} = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C _{AD}	V _{IN} = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

LOW CAPACITANCE COFP

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
OE capacitance	C _{OE}	V _{IN} = 0 V, f = 1.0 MHz	32	pF
COFP G4 capacitance	C _{WE}	V _{IN} = 0 V, f = 1.0 MHz	32	pF
\overline{CS} 1-4 capacitance	C _{CS}	V _{IN} = 0 V, f = 1.0 MHz	15	pF
Data I/O capacitance	C _{I/O}	V _{I/O} = 0 V, f = 1.0 MHz	15	pF
Address input capacitance	C _{AD}	V _{IN} = 0 V, f = 1.0 MHz	32	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Units		
			Min	Max	
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10	μA
Output Leakage Current	I _{LO}	\overline{CS} = V _{IH} , \overline{OE} = V _{IH} , V _{OUT} = GND to V _{CC}		10	μA
Operating Supply Current x 32 Mode	I _{CC x 32}	\overline{CS} = V _{IL} , \overline{OE} = V _{IH} , f = 5MHz, V _{CC} = 5.5		200	mA
Standby Current	I _{SB}	\overline{CS} = V _{IH} , \overline{OE} = V _{IH} , f = 5MHz, V _{CC} = 5.5		4.0	mA
Output Low Voltage	V _{OL}	I _{OL} = 2.1mA, V _{CC} = 4.5		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -1.0mA, V _{CC} = 4.5	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} - 0.3V, V_{IL} = 0.3V

DATA RETENTION CHARACTERISTICS

(T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Units			
			Min	Typ	Max	
Data Retention Supply Voltage	V _{DR}	\overline{CS} ≥ V _{CC} - 0.2V	2.0		5.5	V
Data Retention Current	I _{CCDR1}	V _{CC} = 3V		0.4	1.6	mA



AC CHARACTERISTICS

(VCC = 5.0V, VSS = 0V, TA = -55°C to +125°C)

Parameter	Symbol	-70		-85		-100		-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle										
Read Cycle Time	t _{RC}	70		85		100		120		ns
Address Access Time	t _{AA}		70		85		100		120	ns
Output Hold from Address Change	t _{OH}	5		5		5		5		ns
Chip Select Access Time	t _{ACS}		70		85		100		120	ns
Output Enable to Output Valid	t _{OE}		35		40		50		60	ns
Chip Select to Output in Low Z	t _{CLZ} ¹	10		10		10		10		ns
Output Enable to Output in Low Z	t _{OLZ} ¹	5		5		5		5		ns
Chip Disable to Output in High Z	t _{CHZ} ¹		25		25		35		35	ns
Output Disable to Output in High Z	t _{OHZ} ¹		25		25		35		35	ns

1. This parameter is guaranteed by design but not tested.

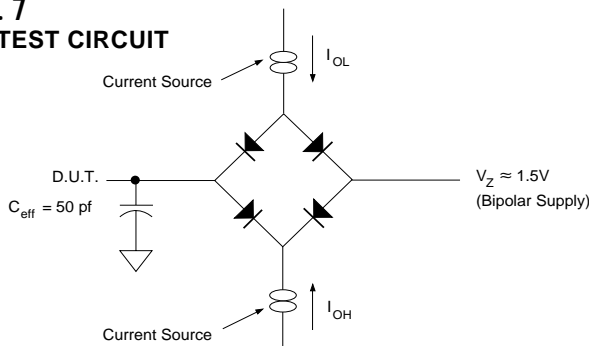
AC CHARACTERISTICS

(VCC = 5.0V, VSS = 0V, TA = -55°C to +125°C)

Parameter	Symbol	-70		-85		-100		-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle										
Write Cycle Time	t _{WC}	70		85		100		120		ns
Chip Select to End of Write	t _{CW}	60		75		80		100		ns
Address Valid to End of Write	t _{AW}	60		75		80		100		ns
Data Valid to End of Write	t _{DW}	30		30		40		40		ns
Write Pulse Width	t _{WP}	50		50		60		60		ns
Address Setup Time	t _{AS}	0		0		0		0		ns
Address Hold Time	t _{AH}	5		5		5		5		ns
Output Active from End of Write	t _{OW} ¹	5		5		5		5		ns
Write Enable to Output in High Z	t _{WHZ} ¹		25		25		35		35	ns
Data Hold from Write Time	t _{DH}	0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.

FIG. 7
AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V _{IL} = 0, V _{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

- V_Z is programmable from -2V to +7V.
- I_{OL} & I_{OH} programmable from 0 to 16mA.
- Tester Impedance Z₀ = 75 Ω.
- V_Z is typically the midpoint of V_{OH} and V_{OL}.
- I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
- ATE tester includes jig capacitance.



FIG. 6
TIMING WAVEFORM - READ CYCLE

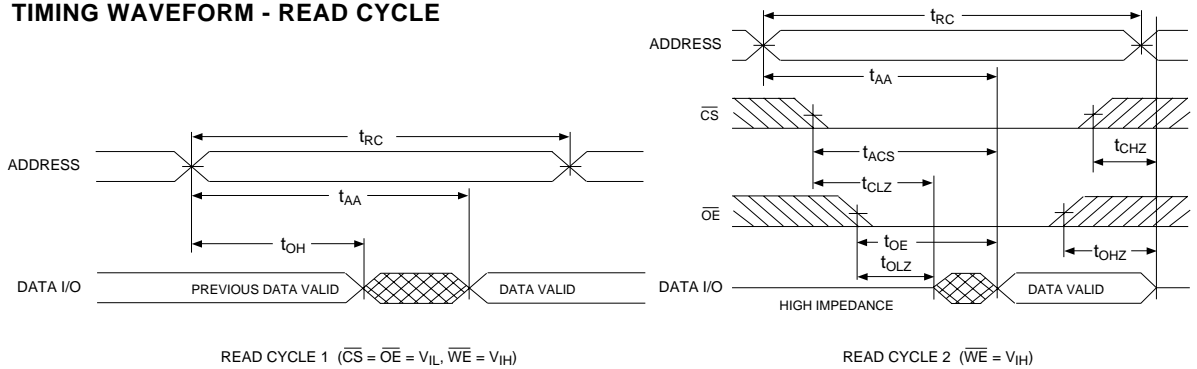


FIG. 7
WRITE CYCLE - \overline{WE} CONTROLLED

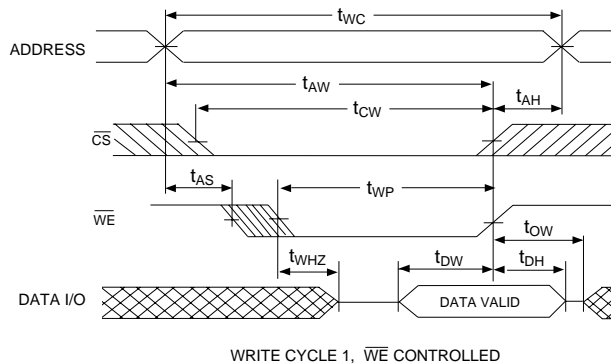
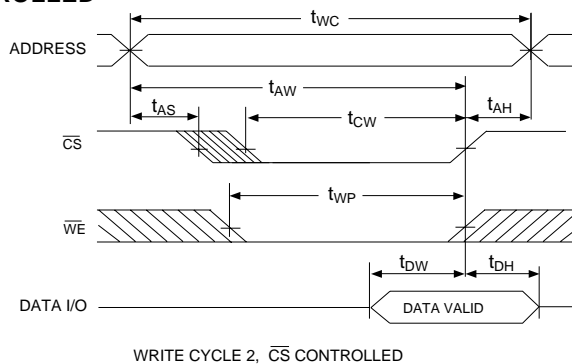
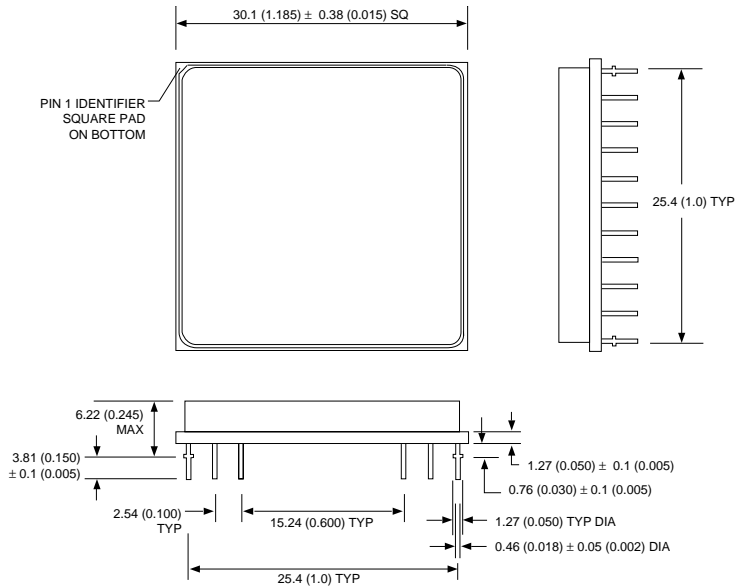


FIG. 8
WRITE CYCLE - \overline{CS} CONTROLLED



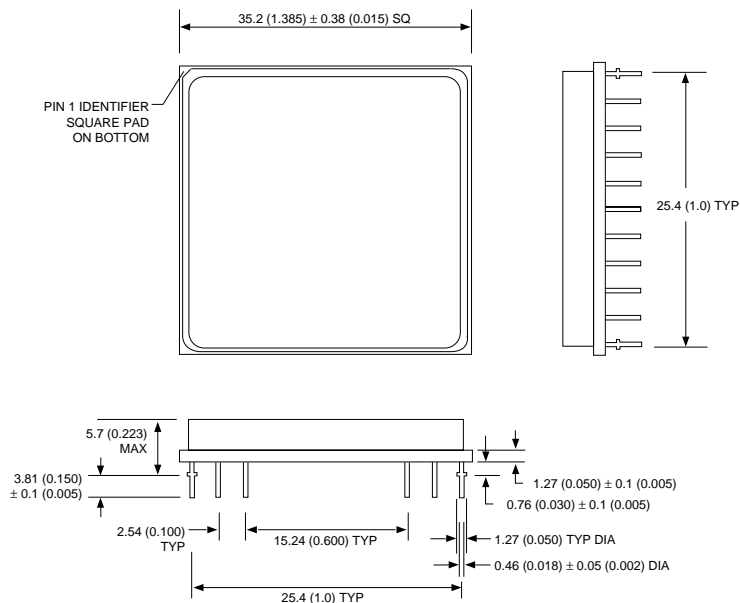


PACKAGE 401: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHEMICALLY IN INCHES

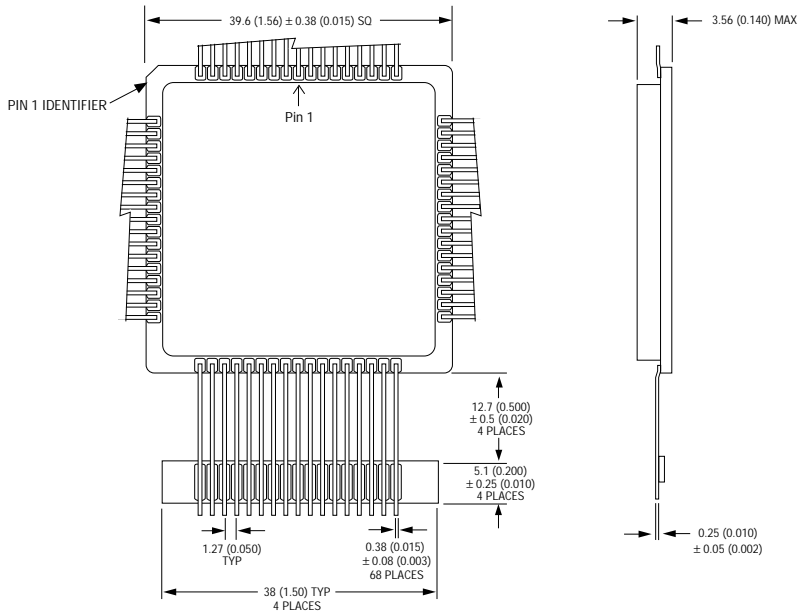
PACKAGE 402: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H2)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHEMICALLY IN INCHES



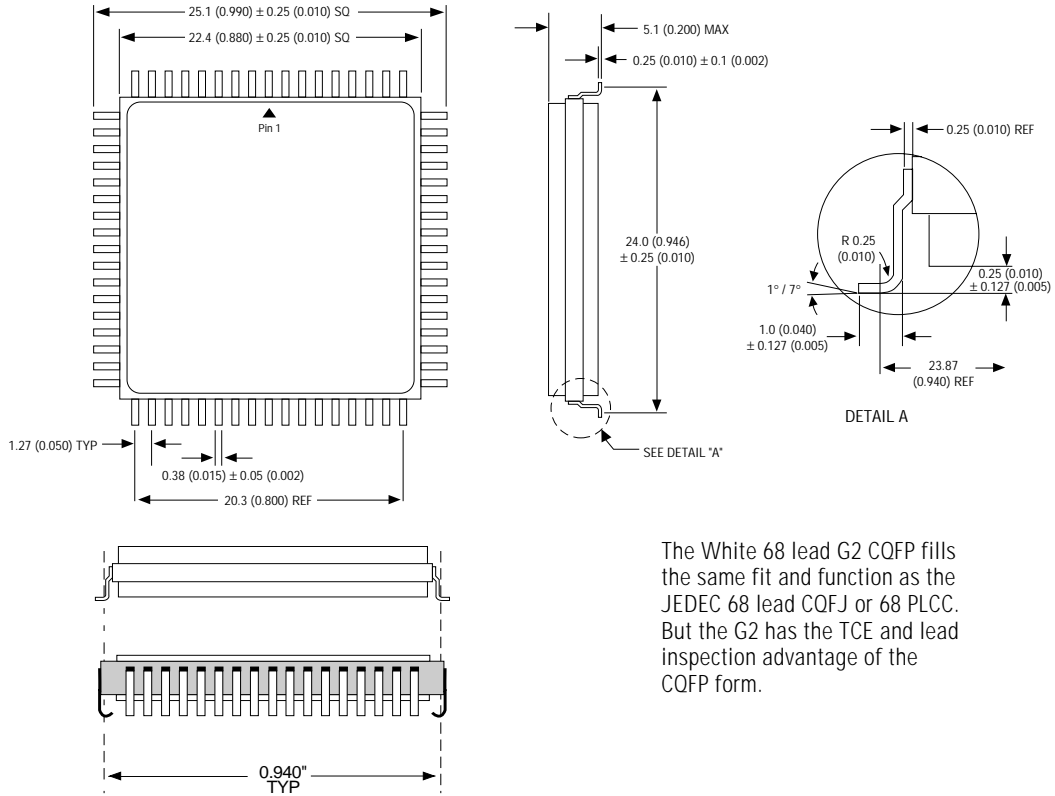
PACKAGE 502: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G4T)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



PACKAGE 500: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2)

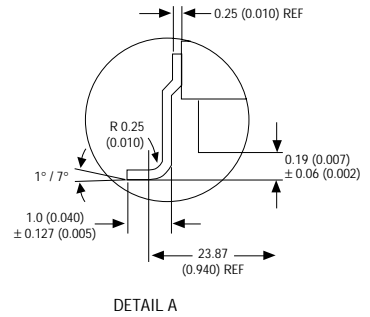
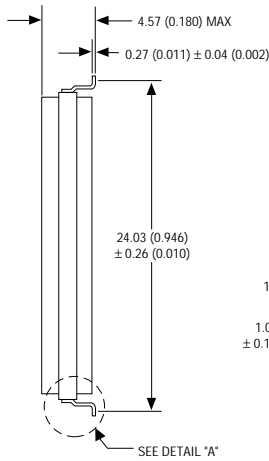
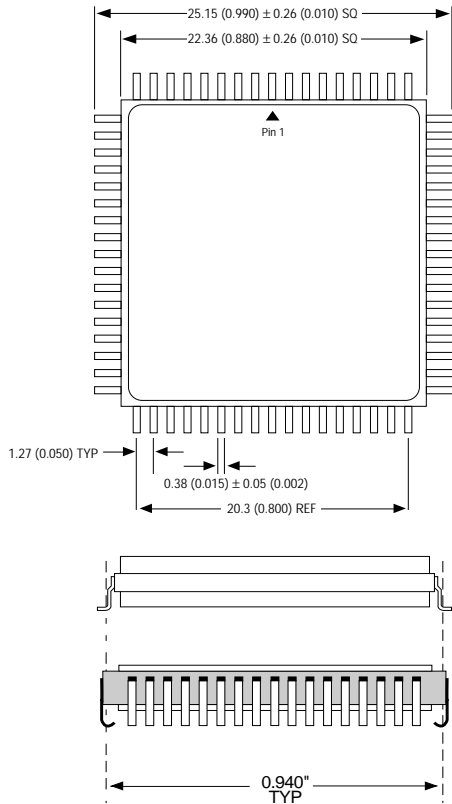


The White 68 lead G2 CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2 has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



PACKAGE 509: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2T)



The White 68 lead G2T CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2T has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



ORDERING INFORMATION

W S 512K 32 X - XXX X X X X

LEAD FINISH:

- Blank = Gold plated leads
- A = Solder dip leads

SPECIAL PROCESSING:

- E = Epitaxial Layer

DEVICE GRADE:

- Q = MIL-STD-883 Compliant
- M = Military Screened -55°C to +125°C
- I = Industrial -40°C to 85°C
- C = Commercial 0°C to +70°C

PACKAGE TYPE:

- H = Ceramic Hex-In-line Package, HIP (Package 401)
- H2 = Ceramic Hex-In-line Package, HIP (Package 402)
- G2 = 22.4mm Ceramic Quad Flat Pack, CQFP (Package 500)
- G2T = 22.4mm Ceramic Quad Flat Pack, Low Profile CQFP (Package 509)
- G4T = 40mm Low Profile CQFP (Package 502)

ACCESS TIME (ns)

IMPROVEMENT MARK:

- N = No Connect at pin 21 and 39 in HIP for Upgrades
- F = Low Capacitance CQFP

ORGANIZATION, 512Kx32

- User configurable as 1Mx16 or 2Mx8

SRAM

WHITE MICROELECTRONICS



DEVICE TYPE	SPEED	PACKAGE	SMD NO.
512K x 32 SRAM Module	120ns	66 pin HIP (H)	5962-94611 01H_X
512K x 32 SRAM Module	100ns	66 pin HIP (H)	5962-94611 02H_X
512K x 32 SRAM Module	85ns	66 pin HIP (H)	5962-94611 03H_X
512K x 32 SRAM Module	70ns	66 pin HIP (H)	5962-94611 04H_X
512K x 32 SRAM Module	120ns	66 pin HIP (H2)	5962-94611 01HXX
512K x 32 SRAM Module	100ns	66 pin HIP (H2)	5962-94611 02HXX
512K x 32 SRAM Module	85ns	66 pin HIP (H2)	5962-94611 03HXX
512K x 32 SRAM Module	70ns	66 pin HIP (H2)	5962-94611 04HXX
512K x 32 SRAM Module	120ns	68 pin CQFP Low Profile (G4T)	5962-94611 01HZX
512K x 32 SRAM Module	100ns	68 pin CQFP Low Profile (G4T)	5962-94611 02HZX
512K x 32 SRAM Module	85ns	68 pin CQFP Low Profile (G4T)	5962-94611 03HZX
512K x 32 SRAM Module	70ns	68 pin CQFP Low Profile (G4T)	5962-94611 04HZX
512K x 32 SRAM Module	120ns	68 pin CQFP/J (G2)	5962-94611 01HMX
512K x 32 SRAM Module	100ns	68 pin CQFP/J (G2)	5962-94611 02HMX
512K x 32 SRAM Module	85ns	68 pin CQFP/J (G2)	5962-94611 03HMX
512K x 32 SRAM Module	70ns	68 pin CQFP/J (G2)	5962-94611 04HMX
512K x 32 SRAM Module	120ns	68 lead CQFP/J (G2T)	5962-94611 01HMX
512K x 32 SRAM Module	100ns	68 lead CQFP/J (G2T)	5962-94611 02HMX
512K x 32 SRAM Module	85ns	68 lead CQFP/J (G2T)	5962-94611 03HMX
512K x 32 SRAM Module	70ns	68 lead CQFP/J (G2T)	5962-94611 04HMX